19-5303; Rev 0; 6/10

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

MAX2063

General Description

The MAX2063 high-linearity, dual digital variable-gain amplifier (VGA) operates in the 50MHz to 1000MHz frequency range. Each digital attenuator is controlled as a slave peripheral using either the SPI™-compatible interface or a 5-bit parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows "rapid-fire" gain selection between each of four steps, preprogrammed by the user through the SPI-compatible interface. A separate 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus.

Since each of the stages has its own external RF input and RF output, this component can be configured to either optimize noise figure (amplifier configured first) or OIP3 (amplifier configured last). The device's performance features include 24dB of amplifier gain (amplifier only), 5.6dB noise figure (NF) at maximum gain (including attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

In addition, the device operates from a single +5V supply with full performance, or a +3.3V supply for an enhanced power-savings mode with lower performance. This device is available in a compact 48-pin thin QFN package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range, from T_C = -40°C to +85°C.

Applications

- IF and RF Gain Stages
- Temperature-Compensation Circuits
- Cellular Band WCDMA and cdma2000® Base Stations
- GSM 850/GSM 900 EDGE Base Stations
- WiMAX™ and LTE Base Stations and Customer Premise Equipment
- Fixed Broadband Wireless Access
- Wireless Local Loop
- Military Systems

Features

- ♦ **Independently Controlled Dual Paths**
- ♦ **50MHz to 1000MHz RF Frequency Range**
- ♦ **Pin-Compatible Family Includes**
  - **MAX2062 (Analog/Digital VGA)**
  - **MAX2064 (Analog-Only VGA)**
- ♦ **21.3dB (typ) Maximum Gain**
- ♦ **0.25dB Gain Flatness Over 100MHz Bandwidth**
- ♦ **31dB Gain Range**
- ♦ **58dB Path Isolation at 200MHz**
- ♦ **Supports Four "Rapid-Fire" Preprogrammed Attenuator States**
  - **Quickly Access Any One of Four Customized Attenuation States Without Reprogramming the SPI Bus**
  - **Ideal for Fast-Attack, High-Level Blocker Protection**
  - **Prevents ADC Overdrive Condition**
- ♦ **Excellent Linearity at 200MHz**
  - **+41dBm OIP3**
  - **+56dBm OIP2**
  - **+19dBm Output 1dB Compression Point**
- ♦ **5.6dB Typical Noise Figure**
- ♦ **25ns Digital Switching Time**
- ♦ **Very Low Distortion VGA Amplitude Overshoot/ Undershoot of 0.05dB**
- ♦ **Single +5V Supply (or +3.3V Operation)**
- ♦ **Amplifier Power-Down Mode for TDD Applications**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2063ETM+	-40°C to +85°C	48 Thin QFN-EP*
MAX2063ETM+T	-40°C to +85°C	48 Thin QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

SPI is a trademark of Motorola, Inc.
cdma2000 is a registered trademark of Telecommunications Industry Association.
WiMAX is a trademark of WiMAX Forum.

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ABSOLUTE MAXIMUM RATINGS

$V_{CC_AMP_1}$, $V_{CC_AMP_2}$, V_{CC_RG} to GND ....-0.3V to +5.5V
STA_A_1, STA_A_2, STA_B_1, STA_B_2, PD_1, PD_2, AMPSET to GND ....-0.3V to +3.6V
DAT, $\overline{CS}$, CLK, DA_SP to GND ....-0.3V to +3.6V
D0_1, D1_1, D2_1, D3_1, D4_1, D0_2, D1_2, D2_2, D3_2, D4_2 to GND ....-0.3V to +3.6V
AMP_IN_1, AMP_IN_2 to GND.........................+0.95V to +1.2V
AMP_OUT_1, AMP_OUT_2 to GND ....-0.3V to +5.5V
D_ATT_IN_1, D_ATT_IN_2, D_ATT_OUT_1, D_ATT_OUT_2 to GND..0V to +3.6V
REG_OUT to GND...-0.3V to +3.6V
RF Input Power (D_ATT_IN_1, D_ATT_IN_2) .... +20dBm
RF Input Power (AMP_IN_1, AMP_IN_2)..................... +18dBm
θ_{JC} (Notes 1, 2)... +12.3°C/W
θ_{JA} (Notes 2, 3)... +38°C/W
Continuous Power Dissipation (Note 1) 5.3W
Operating Case Temperature Range (Note 4) .. -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = +4.75V to +5.25V, AMPSET = 0, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC_}$ = +5.0V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{DC}			148	205	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		5.2	8	mA
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		1.7		3.465	V
Input Logic Current	I_{IH}, I_{IL}		-1		+1	µA

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = +3.135V to +3.465V, AMPSET = 1, PD_1 = PD_2 = 0, T_C = -40°C to +85°C. Typical values are at $V_{CC_}$ = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.135	3.3	3.465	V
Supply Current	I_{DC}			88	145	mA
Power-Down Current	I_{DCPD}	PD_1 = PD_2 = 1, V_{IH} = 3.3V		4.3	8	mA
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		1.7		3.465	V

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 5)	50		1000	MHz

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G	f_{RF} = 50MHz		22.0		dB
		f_{RF} = 100MHz		21.7		
		f_{RF} = 200MHz		21.3		
		f_{RF} = 350MHz, T_C = +25°C	18	21.0	23	
		f_{RF} = 450MHz		20.8		
		f_{RF} = 750MHz		19.9		
		f_{RF} = 900MHz		18.3		
Gain vs. Temperature				-0.006		dB/°C
Gain Flatness vs. Frequency		From 100MHz to 200MHz		0.35		dB
		Any 100MHz frequency band from 200MHz to 500MHz		0.25		
Noise Figure	NF	f_{RF} = 50MHz		5.2		dB
		f_{RF} = 100MHz		5.4		
		f_{RF} = 200MHz		5.6		
		f_{RF} = 350MHz		5.8		
		f_{RF} = 450MHz		5.9		
		f_{RF} = 750MHz		6.4		
		f_{RF} = 900MHz		6.7		
Total Attenuation Range				30.8		dB
Output Second-Order Intercept Point (Minimum Attenuation)	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$		51.6		dBm
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.8		dB
		RF input 2 amplified power measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		49.4		

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+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 50MHz			47.1		dBm
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 100MHz			43.9		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 200MHz			41.0		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 350MHz			37.0		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 450MHz			35.2		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 750MHz			28.7		
		P_{OUT} = 0dBm/tone, Δf = 1MHz, f_{RF} = 900MHz			26.5		
Output -1dB Compression Point	P_{1dB}	(Note 7)			18.8		dBm
Second Harmonic	HD2	P_{OUT} = +3dBm			-54.8		dBc
Third Harmonic	HD3	P_{OUT} = +3dBm			-72.9		dBc
Group Delay		Includes EV kit PCB delays			0.87		ns
Amplifier Power-Down Time		PD_1 or PD_2 from 0 to 1, amplifier DC supply current settles to within 0.1mA			0.5		µs
Amplifier Power-Up Time		PD_1 or PD_2 from 1 to 0, amplifier DC supply current settles to within 1%			0.5		µs
Input Return Loss	RL_{IN}	50Ω source			23.3		dB
Output Return Loss	RL_{OUT}	50Ω load			24.4		dB
DIGITAL ATTENUATOR (each path, unless otherwise noted)							
Insertion Loss	IL				3.0		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$			53.1		dBm
Input Third-Order Intercept Point	IIP3	P_{IN1} = 0dBm, P_{IN2} = 0dBm (minimum attenuation), Δf = 1MHz			43.2		dBm
Attenuation Range					30.8		dB
Step Size					1		dB
Relative Attenuation Accuracy					0.11		dB
Absolute Attenuation Accuracy					0.23		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		-0.4		Degrees
			0dB to 24dB		0.6		
			0dB to 31dB		0.9		

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = +4.75V to +5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = +5.0V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Amplitude Overshoot/ Undershoot		Between any two states	Elapsed time = 15ns		1.0		dB
			Elapsed time = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss	RL_{IN}	50Ω source			21.6		dB
Output Return Loss	RL_{OUT}	50Ω load			21.2		dB
SERIAL PERIPHERAL INTERFACE (SPI)							
Maximum Clock Speed	f_{CLK}				20		MHz
Data-to-Clock Setup Time	t_{CS}				2		ns
Data-to-Clock Hold Time	t_{CH}				2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}				3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}				7		ns
$\overline{CS}$ Setup Time	t_{EWS}				3.5		ns
Clock Pulse Width	t_{CW}				5		ns

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = +3.3V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, 100MHz ≤ f_{RF} ≤ 500MHz, T_C = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = +3.3V, P_{IN} = -20dBm, f_{RF} = 350MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G			20.9		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone		29.6		dBm
Noise Figure	NF			5.9		dB
Total Attenuation Range				30.8		dB
Path Isolation		RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω		48.8		dB
		RF input 2 amplified power measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω		49.1		
Output -1dB Compression Point	P_{1dB}	(Note 7)		13.4		dBm

Note 5: Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*.

Note 6: All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

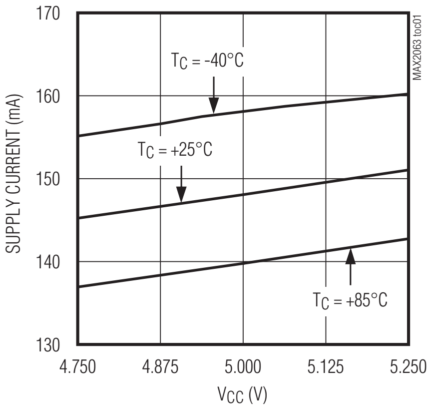
Note 7: It is advisable not to continuously operate RF input 1 or RF input 2 above +15dBm.

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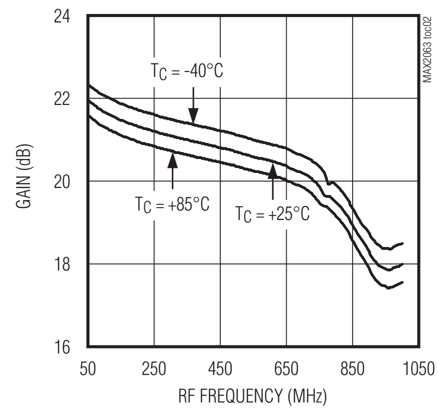
Typical Operating Characteristics

(*Typical Application Circuit*, $\mathbf{V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG} = 5V}$, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

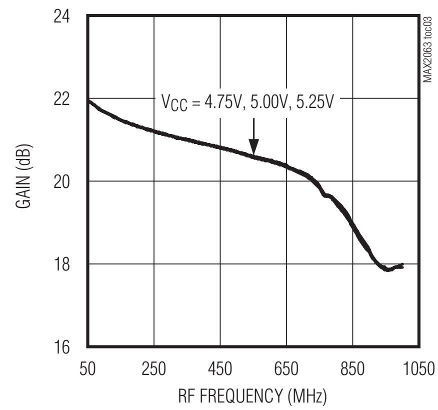
SUPPLY CURRENT vs. V_{CC}



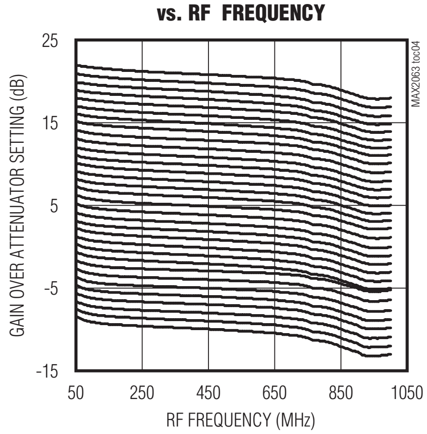
GAIN vs. RF FREQUENCY



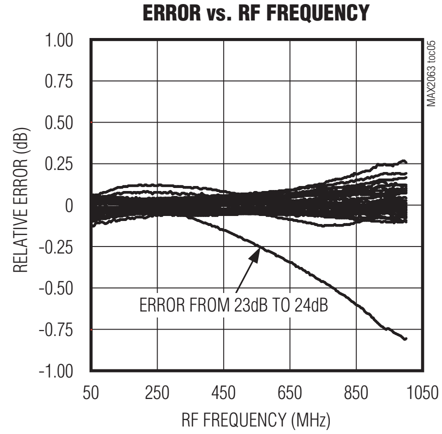
GAIN vs. RF FREQUENCY



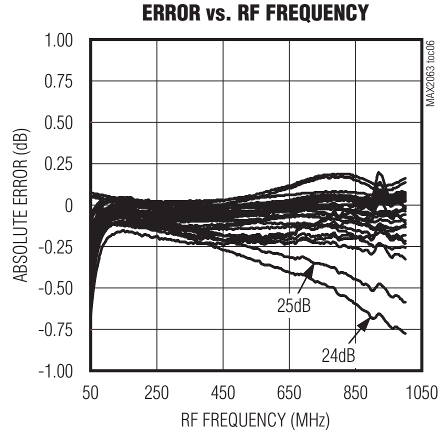
GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



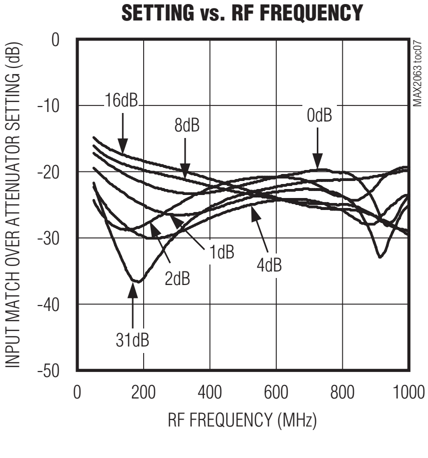
ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



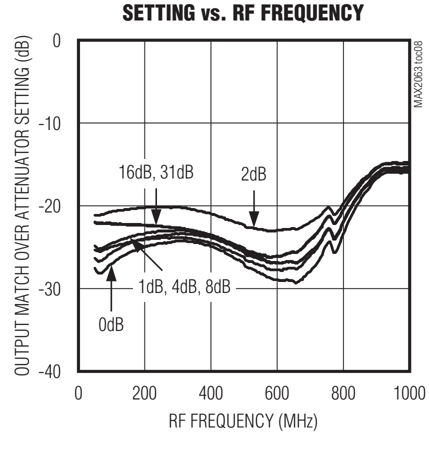
ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY

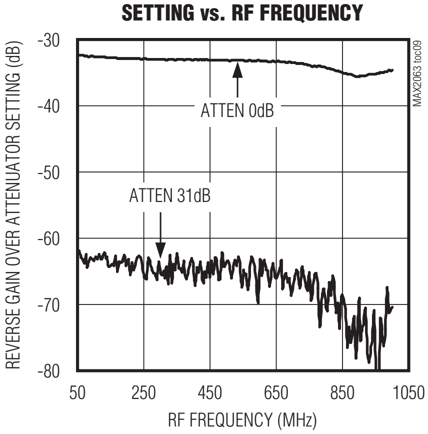


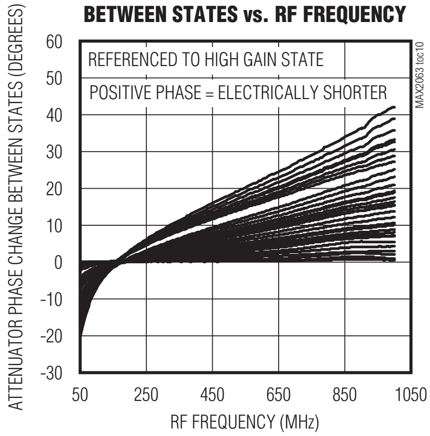
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY

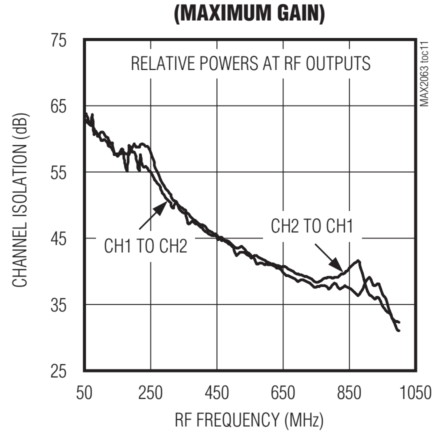


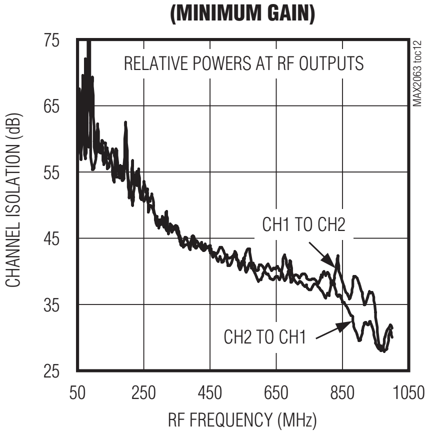
Typical Operating Characteristics (continued)

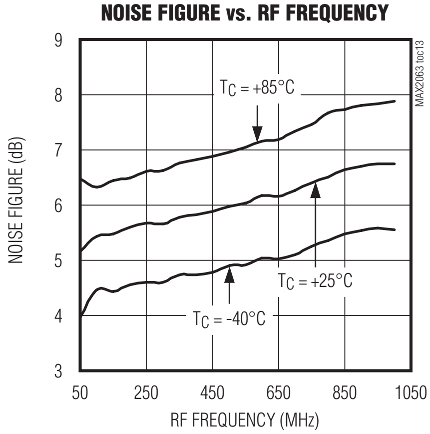
(*Typical Application Circuit*, **V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

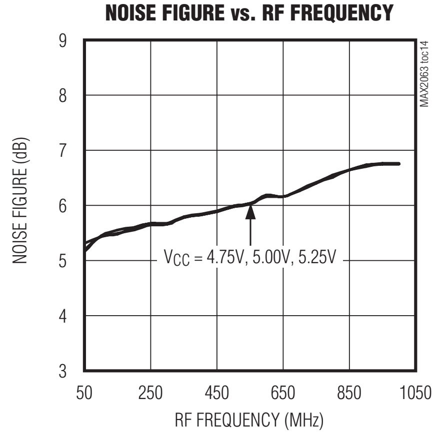


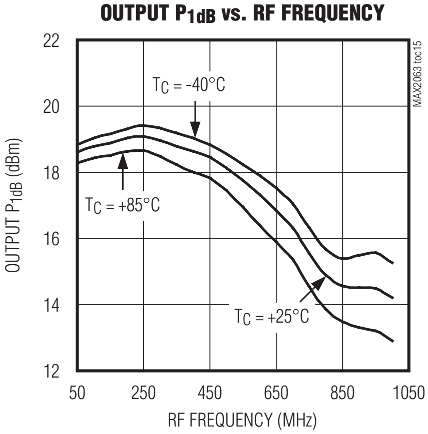


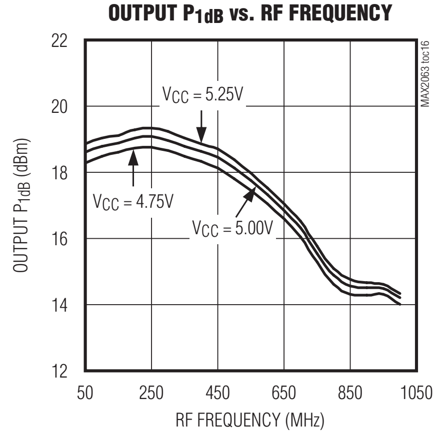










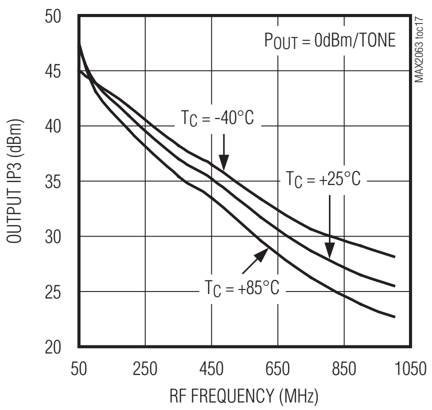


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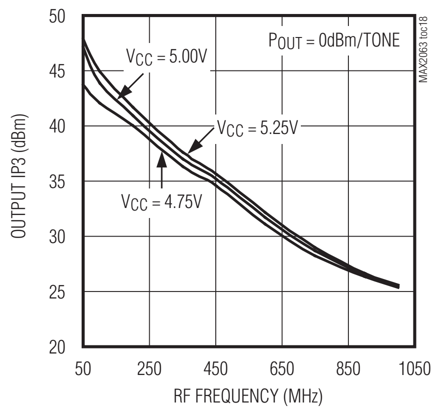
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **$V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

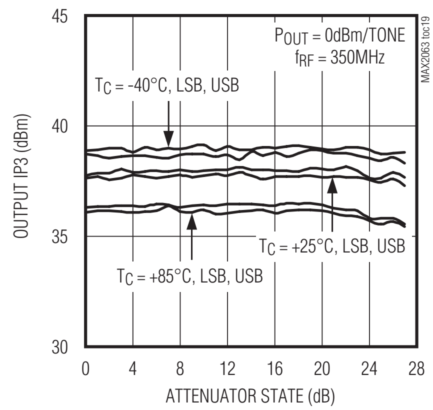
OUTPUT IP3 vs. RF FREQUENCY



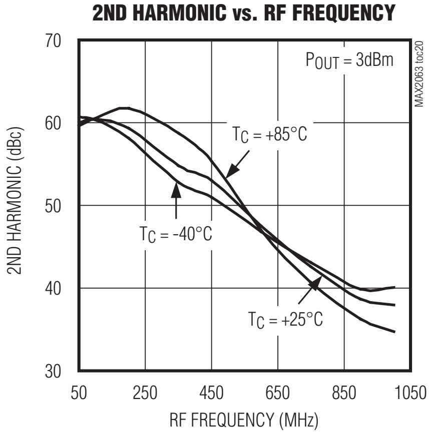
OUTPUT IP3 vs. RF FREQUENCY



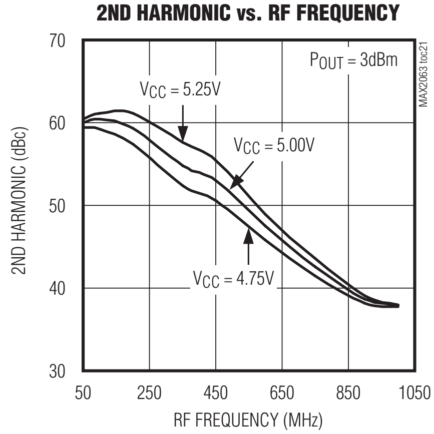
OUTPUT IP3 vs. ATTENUATOR STATE



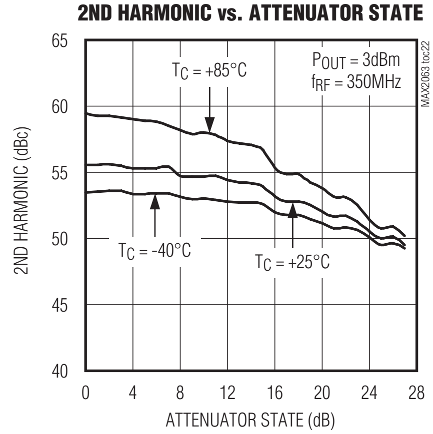
2ND HARMONIC vs. RF FREQUENCY



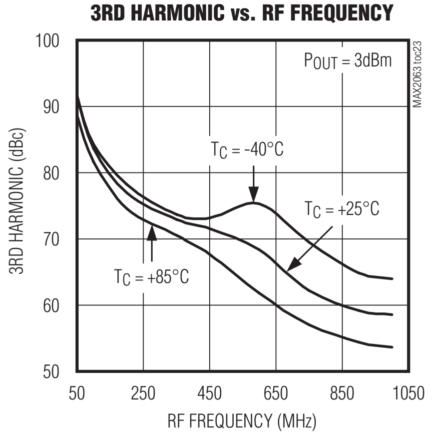
2ND HARMONIC vs. RF FREQUENCY



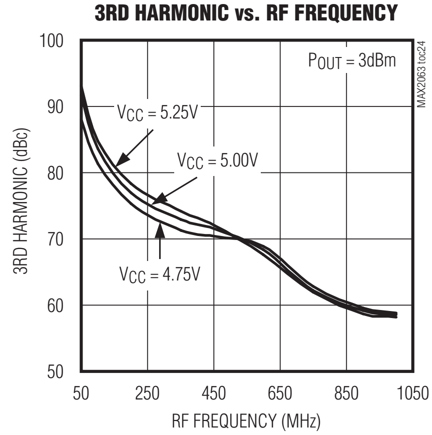
2ND HARMONIC vs. ATTENUATOR STATE



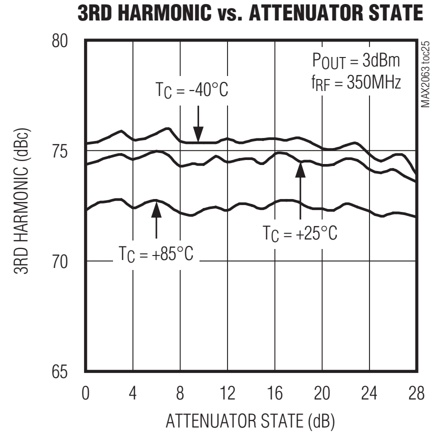
3RD HARMONIC vs. RF FREQUENCY



3RD HARMONIC vs. RF FREQUENCY

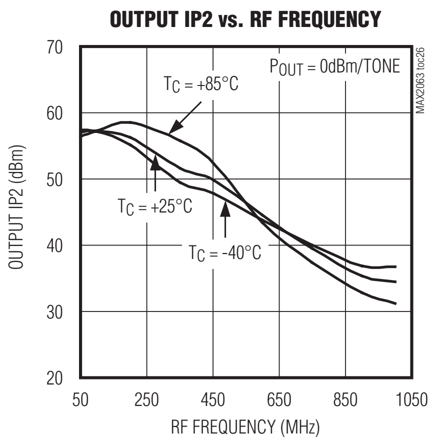


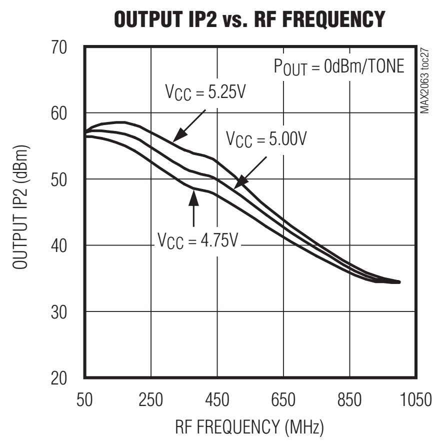
3RD HARMONIC vs. ATTENUATOR STATE

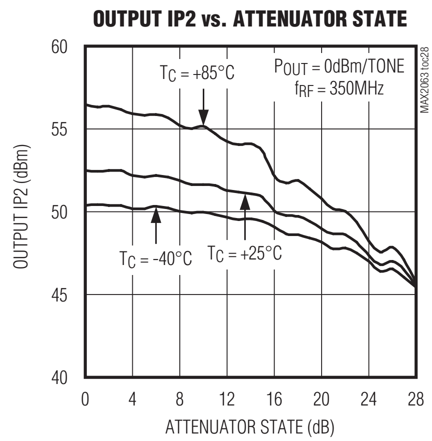


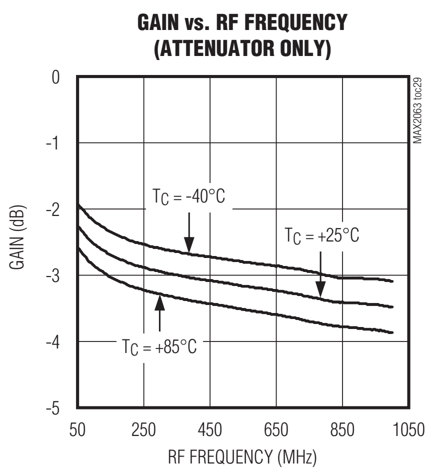
Typical Operating Characteristics (continued)

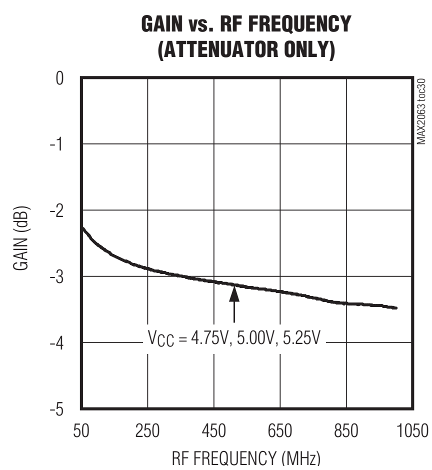
(*Typical Application Circuit*, **$V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = 5V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)









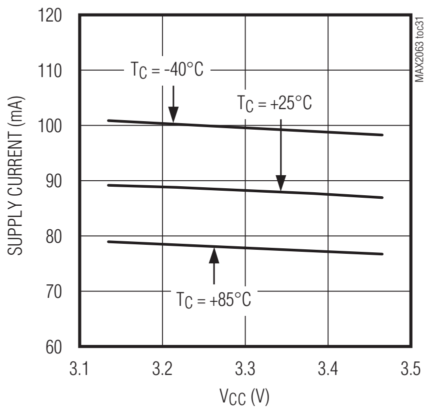


Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

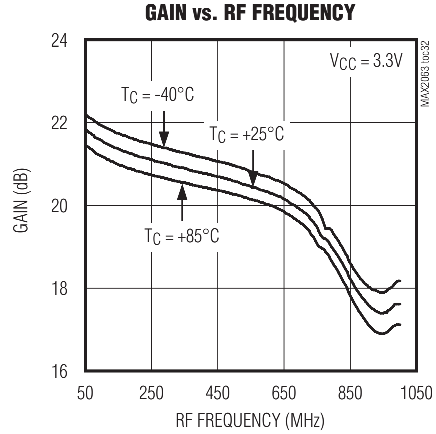
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

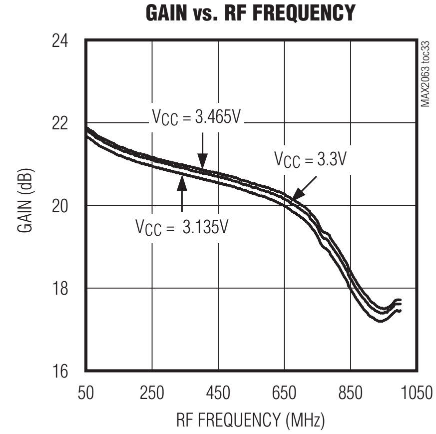
SUPPLY CURRENT vs. V_{CC}



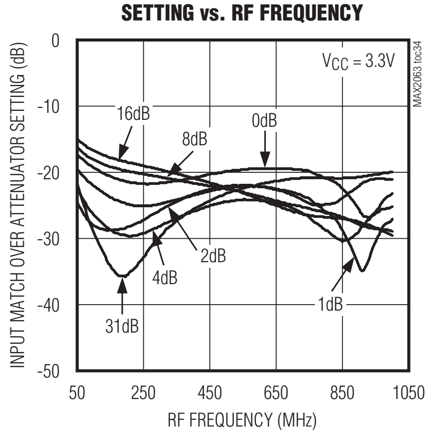
GAIN vs. RF FREQUENCY



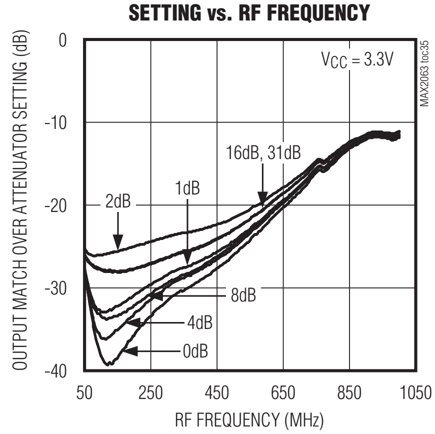
GAIN vs. RF FREQUENCY



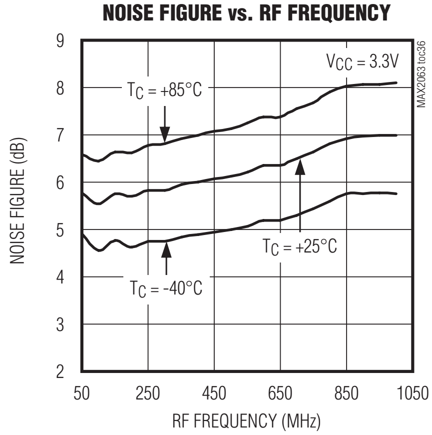
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



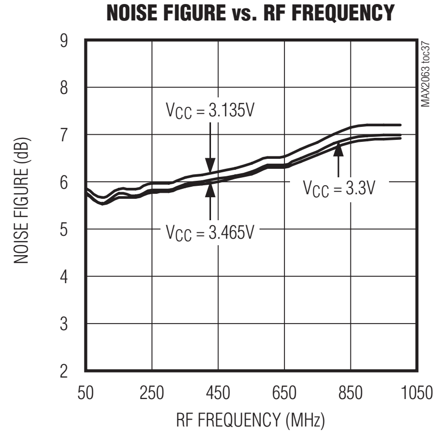
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



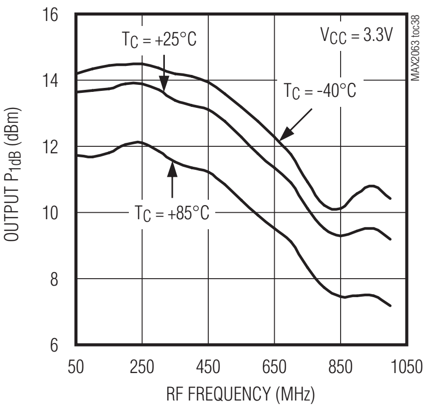
NOISE FIGURE vs. RF FREQUENCY



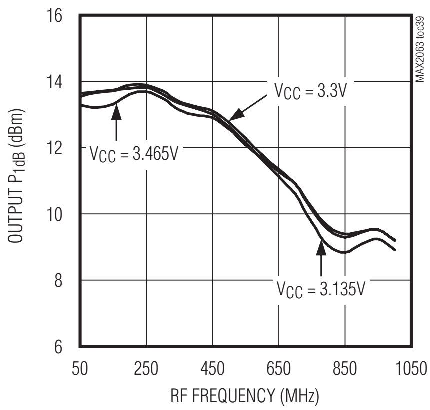
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

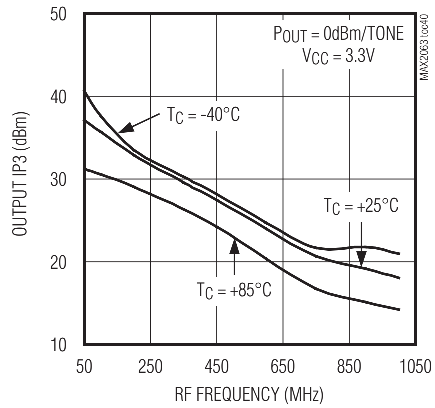
OUTPUT P_{1dB} vs. RF FREQUENCY



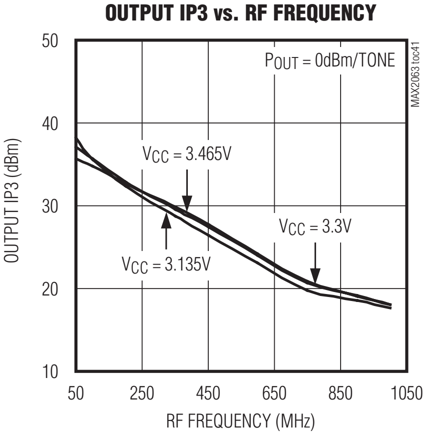
OUTPUT P_{1dB} vs. RF FREQUENCY



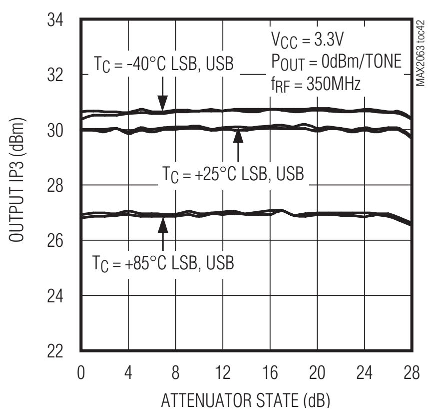
OUTPUT IP3 vs. RF FREQUENCY



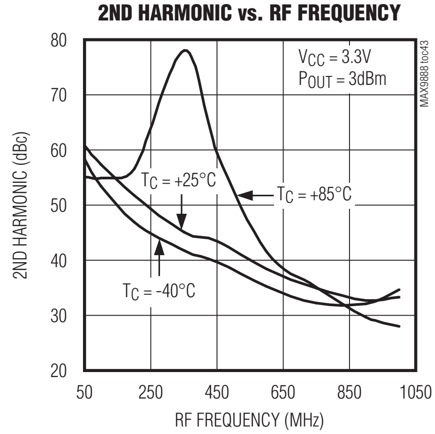
OUTPUT IP3 vs. RF FREQUENCY



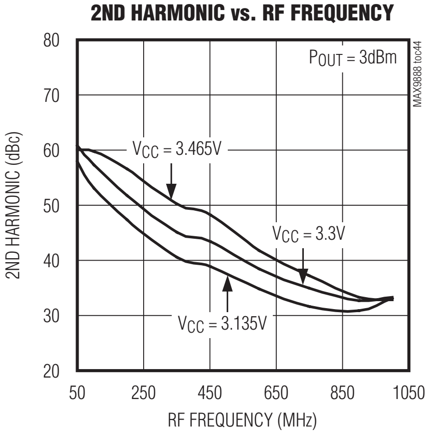
OUTPUT IP3 vs. ATTENUATOR STATE



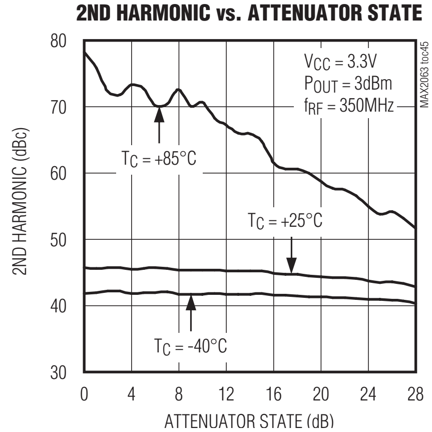
2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. RF FREQUENCY



2ND HARMONIC vs. ATTENUATOR STATE

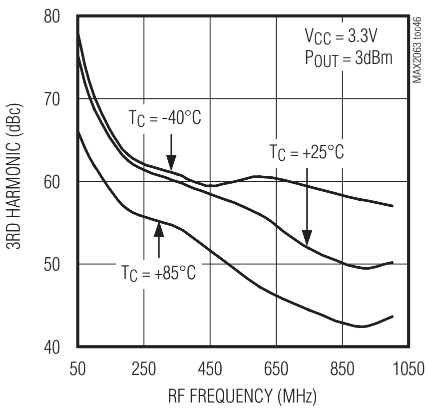


Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

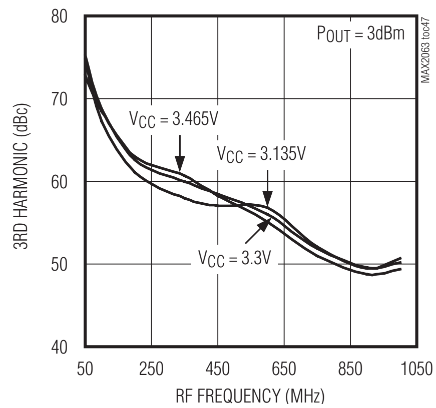
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = V_{CC_RG} = 3.3V**, attenuators are set for maximimum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, P_{IN} = -20dBm, f_{RF} = 350MHz, T_C = +25°C, unless otherwise noted.)

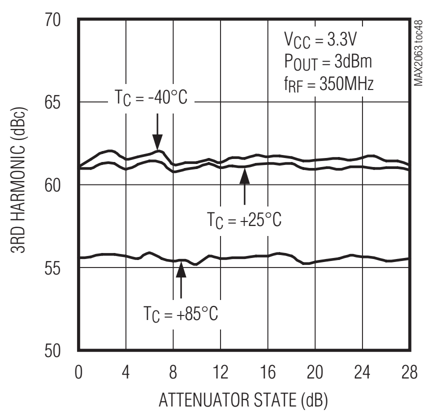
3RD HARMONIC vs. RF FREQUENCY



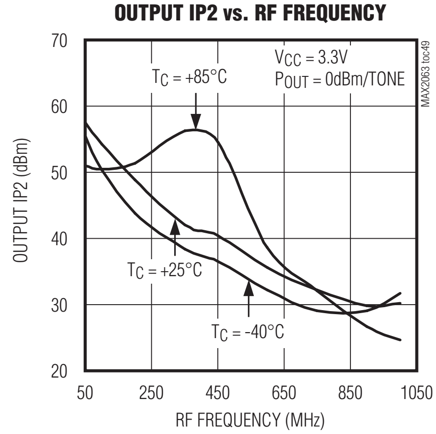
3RD HARMONIC vs. RF FREQUENCY



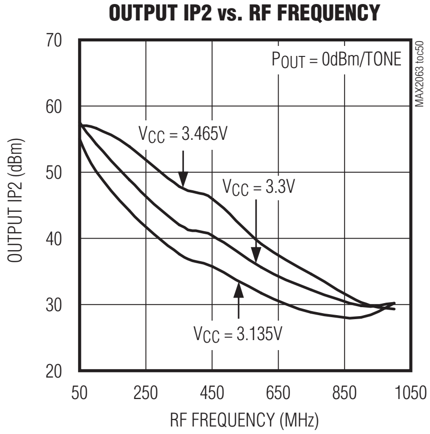
3RD HARMONIC vs. ATTENUATOR STATE



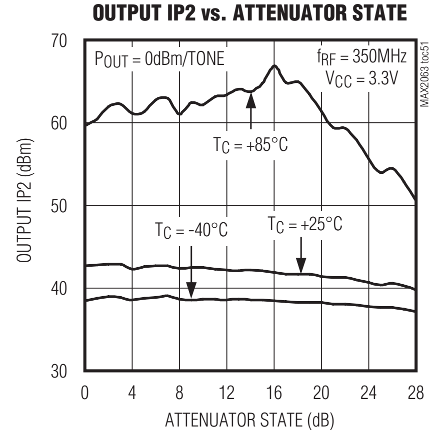
OUTPUT IP2 vs. RF FREQUENCY



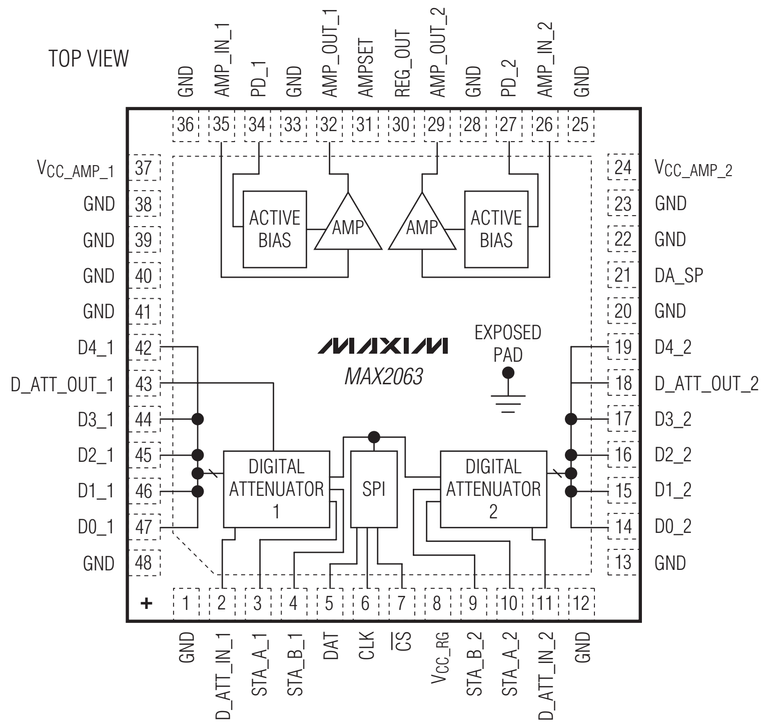
OUTPUT IP2 vs. RF FREQUENCY



OUTPUT IP2 vs. ATTENUATOR STATE



Pin Configuration



THIN QFN
(7mm x 7mm)

Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 20, 22, 23, 25, 28, 33, 36, 38–41, 48	GND	Ground
2	D_ATT_IN_1	5-Bit Digital Attenuator RF Input (50Ω), Path 1. Requires a DC-blocking capacitor.
3	STA_A_1	Digital Attenuator Preprogrammed Attenuation-State Logic Input, Path 1 **State A** / **State B** / **Digital Attenuator 1** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
4	STA_B_1	
5	DAT	SPI Data Digital Input
6	CLK	SPI Clock Digital Input
7	$\overline{CS}$	SPI Chip-Select Digital Input

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Pin Description (continued)

PIN	NAME	FUNCTION
8	V_{CC_RG}	Regulator Supply Input. Connect to a 3.3V or 5V external power supply. V_{CC_RG} powers all circuits except for the driver amplifiers. Bypass with a 10nF capacitor as close as possible to the pin.
9	STA_B_2	Digital Attenuator Preprogrammed Attenuation-State Logic Input, Path 2 **State A** / **State B** / **Digital Attenuator 2** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
10	STA_A_2	
11	D_ATT_IN_2	5-Bit Digital Attenuator RF Input (50Ω), Path 2. Requires a DC-blocking capacitor.
14	D0_2	1dB Attenuator Logic Input, Path 2. Logic 0 = disable, Logic 1 = enable
15	D1_2	2dB Attenuator Logic Input, Path 2. Logic 0 = disable, Logic 1 = enable
16	D2_2	4dB Attenuator Logic Input, Path 2. Logic 0 = disable, Logic 1 = enable
17	D3_2	8dB Attenuator Logic Input, Path 2. Logic 0 = disable, Logic 1 = enable
18	D_ATT_OUT_2	5-Bit Digital Attenuator Output (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to AMP_IN_2 through a 1000pF capacitor.
19	D4_2	16dB Attenuator Logic Input, Path 2. Logic 0 = disable, Logic 1 = enable.
21	DA_SP	Digital Attenuator Serial/Parallel Control Select. Set DA_SP to 1 to select serial control. Set DA_SP to 0 to select parallel control.
24	$V_{CC_AMP_2}$	Driver Amplifier Supply Voltage Input, Path 2. Bypass with a 10nF capacitor as close as possible to the pin.
26	AMP_IN_2	Driver Amplifier Input (50Ω), Path 2. Connect to D_ATT_OUT_2 through a 1000pF capacitor.
27	PD_2	Power-Down, Path 2. See Table 2 for operation details.
29	AMP_OUT_2	Driver Amplifier Output (50Ω), Path 2. Connect a pullup inductor from AMP_OUT_2 to $V_{CC_}$.
30	REG_OUT	Regulator Output. Bypass with a 1µF capacitor.
31	AMPSET	Driver Amplifier Bias Setting for 3.3V Operation. Set to logic 1 for 3.3V on pins V_{CC_AMP1} and V_{CC_AMP2}. Set to logic 0 for 5V.
32	AMP_OUT_1	Driver Amplifier Output (50Ω), Path 1. Connect a pullup inductor from AMP_OUT_1 to $V_{CC_}$.
34	PD_1	Power-Down, Path 1. See Table 2 for operation details.
35	AMP_IN_1	Driver Amplifier Input (50Ω), Path 1. Connect to D_ATT_OUT_1 through a 1000pF capacitor.
37	$V_{CC_AMP_1}$	Driver Amplifier Supply Voltage Input, Path 1. Bypass with a 10nF capacitor as close as possible to the pin.
42	D4_1	16dB Attenuator Logic Input, Path 1. Logic 0 = disable, Logic 1 = enable.
43	D_ATT_OUT_1	5-Bit Digital Attenuator Output (50Ω), Path 1. Requires a DC-blocking capacitor. Connect to AMP_IN_1 through a 1000pF capacitor.
44	D3_1	8dB Attenuator Logic Input, Path 1. Logic 0 = disable, Logic 1 = enable.
45	D2_1	4dB Attenuator Logic Input, Path 1. Logic 0 = disable, Logic 1 = enable.
46	D1_1	2dB Attenuator Logic Input, Path 1. Logic 0 = disable, Logic 1 = enable.
47	D0_1	1dB Attenuator Logic Input, Path 1. Logic 0 = disable, Logic 1 = enable.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large PCB ground plane for proper RF performance and enhanced thermal dissipation.

Detailed Description

The MAX2063 high-linearity digital VGA is a general-purpose, high-performance amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range. Each channel of the device integrates one digital attenuator to provide 31dB of total gain control, as well as a driver amplifier optimized to provide high gain, high output IP3, low NF, and low power consumption.

Each digital attenuator is controlled as a slave peripheral using either the SPI-compatible interface or a 5-bit parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows "rapid-fire" gain selection between each of four steps, preprogrammed by the user through the SPI-compatible interface. A separate 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus.

Because each of the two stages in the separate signal paths has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first) or OIP3 (amplifier configured last). The device's performance features include 24dB of amplifier gain (amplifier only), 5.6dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

5-Bit Digital Attenuator Control

The device integrates two 5-bit digital attenuators to achieve a high level of dynamic range. Each digital attenuator has a 31dB control range, a 1dB step size, and can be programmed either through a dedicated 5-bit parallel bus or through the 3-wire SPI. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuators can be used for both static and dynamic power control.

Driver Amplifiers

The device includes two high-performance drivers with a fixed gain of 24dB. Each driver amplifier circuit is optimized for high linearity for the 50MHz to 1000MHz frequency range.

Table 1. Control Logic

DA_SP	DIGITAL ATTENUATOR
0	Parallel controlled
1	SPI controlled (control voltages show up on the parallel control pins)

Table 2. Operating Modes

RESULT	$V_{CC_}$ (V)	AMPSET	PD_1	PD_2
All on	5	0	0	0
	3.3	1	0	0
AMP1 off AMP2 on	5	0	1	0
	3.3	1	1	0
AMP1 on AMP2 off	5	0	0	1
	3.3	1	0	1
All off	5	0	1	1
	3.3	1	1	1

Applications Information

Operating Modes

The device features an optional +3.3V supply voltage operation with reduced linearity performance. The AMPSET pin needs to be biased accordingly in each mode, as listed in Table 2. In addition, the driver amplifiers can be shut down independently to conserve DC power. See the biasing scheme outlined in Table 2 for details.

SPI Interface and Attenuator Settings

The attenuators can be programmed through the 3-wire SPI/MICROWIRE™-compatible serial interface using 5-bit words. Fifty-six bits of data are shifted in MSB first and framed by $\overline{CS}$. The first 28 bits set the first attenuator, and the following 28 bits set the second attenuator. When $\overline{CS}$ is low, the clock is active and data is shifted on the rising edge of the clock. When $\overline{CS}$ transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 3 for details on the SPI data format.

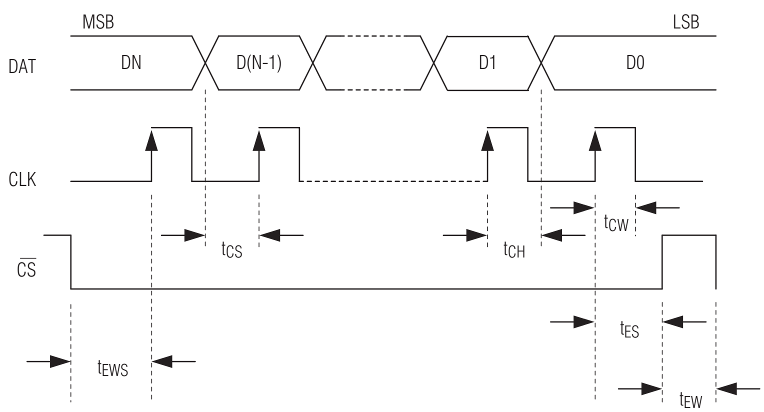
MICROWIRE is a trademark of National Semiconductor Corp.

1st Digital Attenuator Programming

D0:D7	Reserved. Set to logic 0.
D8:D12	Preprogrammed Attenuation State 1 D8 = 1dB bit, D9 = 2dB bit, D10 = 4dB bit, D11 = 8dB bit, D12 = 16dB bit
D13:D17	Preprogrammed Attenuation State 2 D13 = 1dB bit, D14 = 2dB bit, D15 = 4dB bit, D16 = 8dB bit, D17 = 16dB bit
D18:D22	Preprogrammed Attenuation State 3 D18 = 1dB bit, D19 = 2dB bit, D20 = 4dB bit, D21 = 8dB bit, D22 = 16dB bit
D23:D27	Preprogrammed Attenuation State 4 D23 = 1dB bit, D24 = 2dB bit, D25 = 4dB bit, D26 = 8dB bit, D27 = 16dB bit

2nd Digital Attenuator Programming

D28:D35	Reserved. Set to logic 0.
D36:D40	Preprogrammed Attenuation State 1 D36 = 1dB bit, D37 = 2dB bit, D38 = 4dB bit, D39 = 8dB bit, D40 = 16dB bit
D41:D45	Preprogrammed Attenuation State 2 D41 = 1dB bit, D42 = 2dB bit, D43 = 4dB bit, D44 = 8dB bit, D45 = 16dB bit
D46:D50	Preprogrammed Attenuation State 3 D46 = 1dB bit, D47 = 2dB bit, D48 = 4dB bit, D49 = 8dB bit, D50 = 16dB bit
D51:D55	Preprogrammed Attenuation State 4 D51 = 1dB bit, D52 = 2dB bit, D53 = 4dB bit, D54 = 8dB bit, D55 = 16dB bit



NOTES: DATA ENTERED ON CLOCK RISING EDGE.
ATTENUATOR REGISTER STATE CHANGE ON $\overline{CS}$ RISING EDGE.
N = NUMBER OF DATA BITS.

Figure 1. SPI Timing Diagram

Table 3. SPI Data Format

FUNCTION	BIT	DESCRIPTION
2nd Digital Attenuator State 4	D55 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D54	8dB step
	D53	4dB step
	D52	2dB step
	D51	1dB step
2nd Digital Attenuator State 3	D50	16dB step (MSB of the 5-bit word used to program the digital attenuator state 3)
	D49	8dB step
	D48	4dB step
	D47	2dB step
	D46	1dB step
2nd Digital Attenuator State 2	D45	16dB step (MSB of the 5-bit word used to program the digital attenuator state 2)
	D44	8dB step
	D43	4dB step
	D42	2dB step
	D41	1dB step
2nd Digital Attenuator State 1	D40	16dB step (MSB of the 5-bit word used to program the digital attenuator state 1)
	D39	8dB step
	D38	4dB step
	D37	2dB step
	D36	1dB step
Reserved	D35	Bits D[35:28] are reserved. Set to logic 0.
	D34	
	D33	
	D32	
	D31	
	D30	
	D29	
	D28	
1st Digital Attenuator State 4	D27	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step
1st Digital Attenuator State 3	D22	16dB step (MSB of the 5-bit word used to program the digital attenuator state 3)
	D21	8dB step
	D20	4dB step
	D19	2dB step
	D18	1dB step
1st Digital Attenuator State 2	D17	16dB step (MSB of the 5-bit word used to program the digital attenuator state 2)
	D16	8dB step
	D15	4dB step
	D14	2dB step
	D13	1dB step

Table 3. SPI Data Format (continued)

FUNCTION	BIT	DESCRIPTION
1st Digital Attenuator State 1	D12	16dB step (MSB of the 5-bit word used to program the digital attenuator state 1)
	D11	8dB step
	D10	4dB step
	D9	2dB step
	D8	1dB step
Reserved	D7	Bits D[7:0] are reserved. Set to logic 0.
	D6	
	D5	
	D4	
	D3	
	D2	
	D1	
	D0 (LSB)	

Digital Attenuator Settings Using the Parallel Control Bus

To capitalize on its fast 25ns switching capability, the device offers a supplemental 5-bit parallel control interface for each attenuator. The two buses of the digital logic attenuator-control pins (D0_ _–D4_ _) enable the attenuator stages (Table 4).

Direct access to these 5-bit buses enables the user to avoid any programming delays associated with the SPI interface. One of the limitations of any SPI bus is the speed at which commands can be clocked into each peripheral device. By offering direct access to the 5-bit parallel interface, the user can quickly shift between digital attenuator states as needed for critical "fast-attack" automatic gain-control (AGC) applications.

Note that when the digital attenuators are controlled by the SPI bus, the control voltages of each digital attenuator show on the five parallel control pins (pins 14–17, 19 for digital attenuator 2, and pins 42, 44–47 for digital attenuator 1). When the digital attenuators are in SPI mode, the parallel control pins must be open.

"Rapid-Fire" Preprogrammed Attenuation States

The device has an added feature that provides "rapid-fire" gain selection between four preprogrammed attenuation steps. As with the supplemental 5-bit buses previously mentioned, this "rapid-fire" gain selection allows the user to quickly access any one of four customized digital attenuation states without incurring the delays associated with reprogramming the device through the SPI bus.

The switching speed is comparable to that achieved using the supplemental 5-bit parallel buses. However, by employing this specific feature, the digital attenuator I/O is further reduced by a factor of either 5 or 2.5 (5 control bits vs. 1 or 2, respectively), depending on the number of states desired.

The user can employ the STA_A_1 and STA_B_1 (STA_A_2 and STA_B_2 for attenuator 2) logic input pins to apply each step as required (see Tables 5 and 6). Toggling just the STA_A_1 pin (1 control bit) yields two preprogrammed attenuation states; toggling both the STA_A_1 and STA_B_1 pins together (2 control bits) yields four preprogrammed attenuation states.

As an example, assume that the AGC application requires a static attenuation adjustment to trim out gain inconsistencies within a receiver lineup. The same AGC circuit can also be called upon to dynamically attenuate an unwanted blocker signal that could desense the receiver and lead to an ADC overdrive condition. In this example, the device would be preprogrammed (through the SPI bus) with two customized attenuation states—one to address the static gain-trim adjustment, the second to counter the unwanted blocker condition.

Toggling just the STA_A_1 control bit enables the user to switch quickly between the static and dynamic attenuation settings with only one I/O pin.

If desired, the user can also program two additional attenuation states by using the STA_B_1 control bit as a second I/O pin. These two additional attenuation settings are useful for software-defined radio applications where multiple static gain settings are needed to account for different frequencies of operation, or where multiple dynamic attenuation settings are needed to account for different blocker levels (as defined by multiple wireless standards).

Power-Supply Sequencing

The sequence to be used is:

1) Power supply
2) Control lines

Layout Considerations

The pin configuration of the device is optimized to facilitate a very compact physical layout of the device and its associated discrete components. The exposed pad (EP) of the device's 48-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Table 7 lists typical application circuit component values.

Table 4. Digital Attenuator Settings (Parallel Control, DA_SP = 0)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0_ _	Disable 1dB attenuator	Enable 1dB attenuator
D1_ _	Disable 2dB attenuator	Enable 2dB attenuator
D2_ _	Disable 4dB attenuator	Enable 4dB attenuator
D3_ _	Disable 8dB attenuator	Enable 8dB attenuator
D4_ _	Disable 16dB attenuator	Enable 16dB attenuator

Table 5. Programmed Attenuation State Settings for Attenuator 1 (DA_SP = 1)

STA_A_1	STA_B_1	SETTING FOR DIGITAL ATTENUATOR 1*
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

**Defined by SPI programming bits D8:D27 (see Table 3 for details).*

Table 6. Programmed Attenuation State Settings for Attenuator 2 (DA_SP = 1)

STA_A_2	STA_B_2	SETTING FOR DIGITAL ATTENUATOR 2*
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

**Defined by SPI programming bits D36:D55 (see Table 3 for details).*

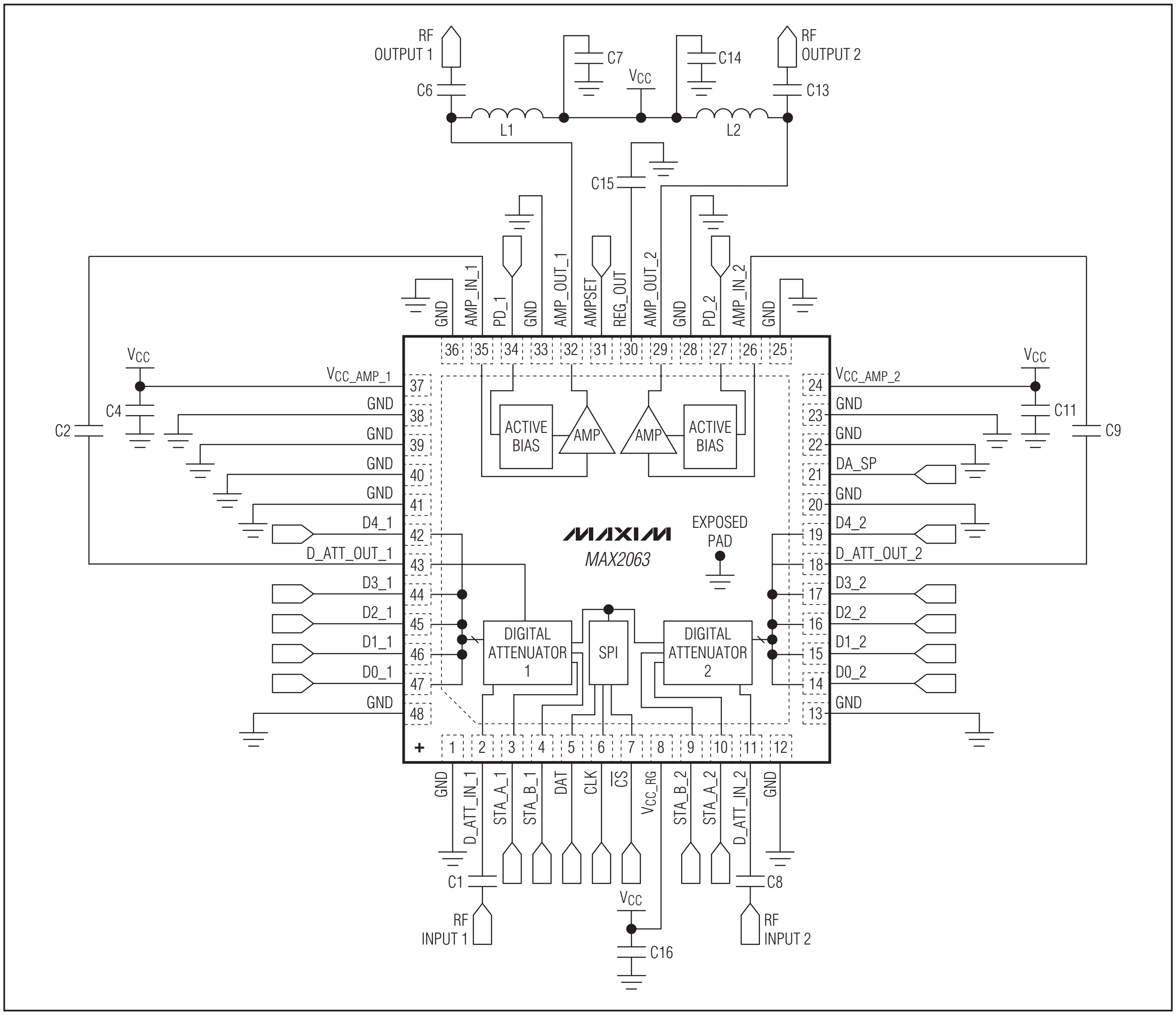
Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Table 7. Typical Application Circuit Component Values

DESIGNATION	QTY	DECRIPTION	COMPONENT SUPPLIER
C1, C2, C6, C8, C9, C13	6	1000pF capacitors (0402) Murata GRM1555C1H102J	Murata North America Electronics, Inc.
C4, C7, C11, C14, C16	5	10nF capacitors (0402) Murata GRM155R71E103K	Murata North America Electronics, Inc.
C15	1	1µF capacitor (0603) Murata GRM188R71C105K	Murata North America Electronics, Inc.
L1, L2	2	820nH inductors (1008) Coilcraft 1008CS-821XJLC	Coilcraft, Inc.
U1	1	VGA (48-pin thin QFN-EP, 7mm x 7mm) Maxim MAX2063ETM+	Maxim Integrated Products, Inc.

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Typical Application Circuit



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 Thin QFN-EP	T4877+7	21-0144	90-0133

Dual 50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—